IN THE CLAIMS:

claims 1-20 are cancelled 8/26/03

21. (Currently Amended) A method of fabricating an EEPROM semiconductor device having a plurality of memory cell transistors, comprising ~~the steps of~~:

~~(a)~~ forming a plurality of field insulating films in parallel with one another in a first direction on a semiconductor substrate, each of said plurality of field insulating films provided for a plurality of memory cell transistors and a plurality of memory transistors formed between two associated adjacent field insulating films;

~~(b)~~ forming a first gate insulating film in each of active regions;

~~(c)~~ forming a plurality of first polysilicon films ~~strips in parallel with one another~~;

E1

~~(d) forming a second gate insulating film and a second polysilicon layer all over the product resulting from said step (c);~~

patterning said first polysilicon film to form first polysilicon strips in parallel with one another, said first polysilicon strips formed in said first direction;

forming a second gate insulating film on said first polysilicon strips

forming a second pllysilicon layer on said second gate insulating film;

~~(e)~~ patterning said second polysilicon layer, said second gate insulating film, ~~and~~ said plurality of first polysilicon strips and said first gate insulating film to ~~thereby~~ form a plurality of control gates, a plurality of second gate insulators, ~~and~~ a plurality of floating gates, ~~said plurality of control gates serving as a plurality of word lines, said plurality of word lines being perpendicular to said plurality of field insulating films and said plurality of first polysilicon strips~~ and a plurality of first gate insulators, respectively;

~~(f)~~ forming drain and source regions;

~~(g)~~ forming a first interlayer insulating layer ~~all over the product resulting from said step (f);~~on an entire surface of said semiconductor substrate;

~~(g')~~ forming contact-holes through said first interlayer insulating layer ~~only above both said drain and source regions in said plurality of memory cell transistors;~~in alignment with said drain and source regions; and

~~(h)~~ forming a first metal wiring layer ~~which is patterned so as to form both a common source line extending in parallel with said plurality of word lines and connecting source regions to one another and a plurality of bit studs extending to said drain regions,~~

~~said first metal wiring layer being formed above a surface of said first interlayer insulating layer;~~on said first interlayer insulating layer and filing said contact-holes therewith to couple said first wiring layer to a corresponding one of said drain and source regions in a memory area and a wiring layer of a logic area.

~~(i) forming a second interlayer insulating layer all over the product resulting from said step (h); and~~

~~(j) forming a second metal wiring layer which is patterned so as to form a bit line extending perpendicularly to said plurality of word lines and connecting said drain regions with each other, said bit line having a top portion and a bottom portion with said top portion being wider than said bottom portion,~~

~~wherein said bottom portion of said bit line is connected to a top portion of said plurality of bit studs and a bottom portion of said plurality of bit studs is connected to said drain regions,~~

~~said first metal wiring layer completely filling said contact holes formed above said drain and source regions, portions of said first metal wiring layer having a width wider than a diameter of said contact holes,~~

~~said first metal wiring layer extends in parallel with said plurality of field insulating films and offset from said plurality of field insulating films such that said first metal wiring layer does not make contact with said plurality of field insulating films, and~~

~~said first metal wiring layer forms a continuous portion connecting ones of said plurality of contact holes formed above said source regions, and forms isolated island regions above ones of said plurality of contact holes formed above said drain regions.~~

22.(Original) The method as set forth in claim 21, wherein said second gate insulating film has a three-layered structure of oxide/nitride/oxide films.

23.(Original) The method as set forth in claim 21, wherein said first and second metal wiring layers are composed of aluminum.

24. (Currently Amended) A method of fabricating an EEPROM semiconductor device having a plurality of memory cell transistors, comprising ~~the steps of~~:

~~(a)~~ forming a plurality of field insulating films in parallel with one another in a first direction on a semiconductor substrate, each of said plurality of field insulating films provided for a plurality of memory cell transistors and a plurality of memory transistors formed between two associated adjacent field insulating films;

~~(b)~~ forming a first gate insulating film in each of active regions;

~~(c)~~ forming a plurality of first polysilicon films ~~strips in parallel with one another~~;

~~(d) forming a second gate insulating film and a second polysilicon layer all over the product resulting from said step (c);~~

patterning said first polysilicon film to form first polysilicon strips in parallel with one another, said first polysilicon strips formed in said first direction;

forming a second gate insulating film on said first polysilicon strips

forming a second pllysilicon layer on said second gate insulating film;

E1

~~(e)~~ patterning said second polysilicon layer, said second gate insulating film, ~~and~~ said plurality of first polysilicon strips and said first gate insulating film to ~~thereby~~ form a plurality of control gates, a plurality of second gate insulators, ~~and~~ a plurality of floating gates, ~~said plurality of control gates serving as a plurality of word lines, said plurality of word lines being perpendicular to said plurality of field insulating films and said plurality of first polysilicon strips~~ and a plurality of first gate insulators, respectively;

~~(f)~~ forming drain and source regions;

~~(g)~~ forming a first interlayer insulating layer ~~all over the product resulting from said step (f);~~on an entire surface of said semiconductor substrate;

~~(g')~~ forming contact-holes through said first interlayer insulating layer ~~only above both said drain and source regions in said plurality of memory cell transistors;~~in alignment with said drain and source regions; and

~~(h)~~ forming a first metal wiring layer ~~which is patterned so as to form both a bit line connecting said drain regions to one another, and a plurality of source studs extending in parallel with said plurality of word lines, said plurality of source studs connecting to said source regions, said plurality of source studs having a top portion and a bottom portion with said top portion of said plurality of source studs being wider than said bottom portion of said plurality of source studs, said first metal wiring layer being formed above a surface~~

~~of said first interlayer insulating layer;~~ on said first interlayer insulating layer and filing said contact-holes therewith to couple said first wiring layer to a corresponding one of said drain and source regions in a memory area and a wiring layer of a logic area;

~~(i) forming a second interlayer insulating layer all over the product resulting from said step (h);~~

~~(j)~~ forming a second metal wiring layer which is patterned so as to form a common source line connecting said source regions with each other~~, said common source line having a top portion and a bottom portion with said top portion of said common source line being wider than said bottom portion of said common source line~~; and

~~(k)~~ forming aluminum backing wiring layers connecting to said plurality of control gates, simultaneously with forming said common source line~~,~~

~~wherein said bottom portion of said common source line is connected to said top portion of said plurality of source studs and said bottom portion of said plurality of source studs is connected to said source regions,~~

E1

~~said first metal wiring layer completely filling said contact holes formed above said drain and source regions, portions of said first metal wiring layer having a width wider than a diameter of said contact holes,~~

~~said first metal wiring layer extends in parallel with said plurality of field insulating films and offset from said plurality of field insulating films such that said first metal wiring layer does not make contact with said plurality of field insulating films, and~~

~~said first metal wiring layer forms a continuous portion connecting ones of said plurality of contact holes formed above said source regions, and forms isolated island regions above ones of said plurality of contact holes formed above said drain regions~~.

25. (Cancelled)

26. (Previously Amended) The method as set forth in claim 24, wherein said backing wiring layers are constituted of said second metal wiring layer.